Electronic Version
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Claims

[c1] A method of forming air gaps in a starting structure on a semiconductor substrate comprising:
depositing a first layer comprising a first material on the starting structure;
depositing a second layer comprising a second material on the first layer;
patterning the second layer, resulting in gaps between portions of the second layer; and
subjecting the substrate to a highly oxidizing environment so that the first material will substantially completely decompose into volatile products and the second material will partially decompose leaving a thin membrane layer.

[c2] A method, according to claim 1, wherein:
the first layer is deposited by a spin-on process.

[c3] A method, according to claim 1, wherein:
the second layer is deposited by a spin-on process.

[c4] A method, according to claim 1, wherein:
the first material comprises comprises a polymer based material which is easily decomposed at low temperatures

or in an oxygen plasma.

[c5] A method, according to claim 1, wherein:
the second material comprises comprises a polymer based material which is easily decomposed at low temperatures or in an oxygen plasma, and has a high content of an oxidizable component.

[c6] A method, according to claim 1, wherein:
the second material comprises a resist containing a high composition of silicon (Si), or aluminum (Al) or any metal which forms a strong coherent oxide film upon oxidation .

[c7] A method, according to claim 1, wherein:
the thin membrane comprises an oxide containing a significant amount of carbon.

[c8] A method, according to claim 1, wherein:
the second material is photosensitive, and is patterned using photolithography.

[c9] A method, according to claim 1, wherein:
the starting structure is a wiring layer comprising conductive lines.

[c10] A method, according to claim 9, wherein:
when the second layer is patterned, selected portions of

the second layer are disposed over selected adjacent ones of the conductive lines of the starting structure.

[c11] A method, according to claim 9, wherein:
air gaps between adjacent conductive lines are sealed off by portions of the thin membrane layer.

[c12] A method, according to claim 9, wherein:
the conductive lines are disposed atop an underlying layer; and
there are gaps between adjacent conductive lines; and
the first material fills the gaps and covers the conductive lines.

[c13] A method, according to claim 12, wherein:
when the second layer is patterned, selected ones of the gaps of the second layer are disposed over selected ones of gaps between adjacent ones of the conductive lines of the starting structure.

[c14] A method, according to claim 9, wherein:
the conductive lines are disposed within a dielectric layer;
there are troughs between adjacent conductive lines; and
the first material fills the troughs and covers the conductive lines.

[c15] A method, according to claim 14, wherein:

when the second layer is patterned, selected ones of the gaps of the second layer are disposed over selected ones of the troughs between adjacent ones of the conductive lines of the starting structure.

[c16] A method, according to claim 1, further comprising:
depositing an interlevel dielectric (ILD) on the surface of the substrate.

[c17] An interconnect structure comprising:
a plurality of conductive lines;
air gaps between adjacent conductive lines; and
portions of a thin membrane layer sealing off the air gaps.

[c18] An interconnect structure, according to claim 17, wherein:
the conductive lines are disposed atop an underlying layer.

[c19] An interconnect structure, according to claim 17, wherein:
the conductive lines are disposed within a dielectric layer;
there are troughs between adjacent conductive lines; and
the first material fills the troughs and covers the conductive lines.

[c20] An interconnect structure, according to claim 17, further comprising:

an interlevel dielectric disposed atop the membrane.